REMARKS/ARGUMENTS

Claims 1-21 are pending in the present application, of which claims 1, 8 and 15 are independent. Claims 1, 8 and 15 have been amended herein. Applicants respectfully request reconsideration and allowance of claims 1, 8 and 15.

I. Amendment to the Specification

Applicants thank the Examiner for the suggested new title. As suggested by the Examiner, applicants have changed the title for this application to "MEMORY DEVICE HAVING SIMULTANEOUS READ/WRITE AND REFRESH OPERATIONS WITH COINCIDENT PHASES." Further, the first paragraph of the application has been amended to enter the patent number for U.S. Patent Application No. 10/414,878, a parent application which issued as U.S. Patent No. 6,717,863 on April 6, 2004.

II. Rejection of Claims 1-3, 8-10 and 15-17

Claims 1-3, 8-10 and 15-17 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,007,022 ("Leigh") in view of U.S. Patent No. 5,808,932 ("Irrinki et al.").

In rejecting claim 1, the Office Action states "Leigh discloses, in FIGs. 2 and 3a-3i, a memory circuit comprising: . . . a plurality of sense amplifiers (58, see FIG. 2), wherein each said sense amplifier is coupled to a corresponding one of the columns (22, see FIG. 2) of the memory cells, and is used to read data stored in the memory cells of the corresponding column during read phases of the memory access cycles."

However, applicants submit that the memory circuit architecture/memory access mechanism of Leigh is completely different from that of the present invention. By way of example, Leigh uses a four phase clock to drive sense amplifiers that are different for reading and refreshing cycles. It can be seen in FIG. 2 that a sense amplifier 46 is used in a refresh circuit 40 for reading during refresh cycles, while a read/restore sense amplifier 58 is used in a restore circuit 52 for reading during read cycles. Such use of different sense amplifiers during the refresh cycles and the read/write cycles is also described on column 5, line 41 to column 6, line 11 of Leigh in reference to FIG. 2.

Of course, when different sense amplifiers are used during the refresh cycles than those used during the read cycles, these additional sense amplifiers undesirably occupy space on the memory chip, which otherwise could be used for additional memory and/or to increase the size of the memory chip.

Claim 1 of the present application has been amended to explicitly recite that which was already inherent therein. Claim 1 (as amended) recites, in a relevant portion, "a plurality of sense amplifiers, wherein <u>each said sense amplifier</u> is coupled to a corresponding one of the columns of the memory cells, and <u>is used to read data stored in the memory cells of the corresponding column during read phases of the refresh cycles and the read/write cycles</u>." (<u>Emphasis Added</u>). By using the same sense amplifier to perform reading during both the refresh cycles and read/write cycles, the redundancy to the sense amplifiers is eliminated.

Further, if the memory circuit of Leigh is modified such that each sense amplifier "is used to read data stored in the memory cells of the corresponding column during read phases of the refresh cycles and the read/write cycles," such a memory circuit would not work properly. Hence, such a modification would render the prior art unsatisfactory for its intended purpose, and therefore, there would be no suggestion or motivation to make the proposed modification under MPEP § 2143.01.

Since Leigh discloses a memory architecture and operation that is different from that of claim 1, and there is no suggestion or motivation to combine Leigh with any other references to practice claim 1, claim 1 is not obvious over Leigh in combination with Irrinki et al. and/or any other reference. Therefore, applicants request that the rejection of claim 1 be withdrawn and that it be allowed.

Claims 8 and 15 have been amended to explicitly recite one of the patentably distinguishable features in a similar manner as claim 1.

Claim 8 now recites, in a relevant portion, "A method of refreshing memory cells organized into columns and rows, the memory cells being accessed during memory access cycles, which include refresh cycles and read/write cycles, the method comprising: reading data stored in the memory cells during read phases of the memory access cycles, wherein same sense amplifiers are used to read the memory cells during both the refresh cycles and the read/write cycles." (Emphasis Added).

Claim 15 now recites, in a relevant portion, "A system-on-chip (SOC) device comprising: . . . a memory block comprising: . . . a plurality of sense amplifiers, wherein each said sense amplifier is coupled to a corresponding one of the columns of the memory cells, and is used to read data stored in the memory cells of the corresponding column during read phases of the refresh cycles and the read/write cycles." (Emphasis Added).

For at least the reasons similar to those given in reference to claim 1 (i.e., Leigh discloses a memory architecture having features different from those of claims 8 and 15 and any modification to Leigh towards the claimed invention would render it unsatisfactory for its intended purpose.), claims 8 and 15 are patentably distinguishable over Leigh and Irrinki et al. Therefore, applicants request that the rejection of claims 8 and 15 be withdrawn and that they be allowed.

Since claims 2-3, 9-10 and 16-17 depend, directly or indirectly, from claims 1, 8 and 15, respectively, they incorporate all the terms and limitations of claim 1, 8 or 15, in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 2-3, 9-10 and 16-17 be withdrawn and that they be allowed.

III. Rejection of Claims 2-7, 9-14 and 16-21

Claims 2-7, 9-14 and 16-21 have been rejected as allegedly being unpatentable over Leigh in view of Irrinki et al., and further in view of U.S. Patent No. 6,134,169 ("Tanaka").

Since claims 2-7, 9-14 and 16-21 depend, directly or indirectly, from claims 1, 8 and 15, respectively, they incorporate all the terms and limitations of claim 1, 8 or 15, in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 2-7, 9-14 and 16-21 be withdrawn and that they be allowed.

In view of the foregoing amendments and remarks, applicants respectfully request an early issuance of a patent with claims 1-21. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call applicants' attorney at the number listed below.

Respectfully submitted,
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